Streaming extension of Gen2 communication protocol

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BACKSCATTER COMMUNICATION RESEARCH CONSORTIUM

KEIO UNIVERSITY

1 Overview

This note proposes an extension of ISO/IEC 18000-63 (2015) specification (hereinafter, Gen2)[1] or a new stream of protocol to enable concurrent sensor data streaming from multiple radio frequency (RF) tags with the multiple subcarrier multiple access (MSMA) technology [2] using backscatter technology. The basic composition of the MSMA system comprises a reader/writer (hereinafter, reader) and a group of multiple backscatter tags (Figure 1).

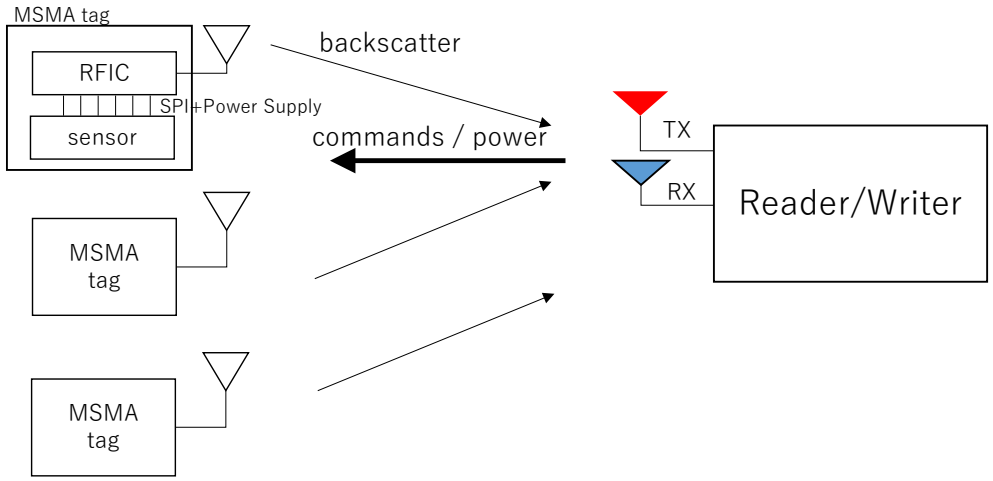

Figure 1 MSMA system composition

As shown in Figure 1, an MSMA tag comprises an RF integrated circuit (RFIC), which handles the communication with the reader, and a sensor connected to RFIC through, for example, the serial peripheral interface (SPI) in our implementation. The power to the sensor can be provided by RFIC, which is the SPI master, and the sensor is an SPI slave.

The concurrency in MSMA in its sensor streaming stage is realized by simultaneously using multiple subcarriers. The Miller encoded subcarrier is extensively used in commercial RFID systems with Gen2 protocol. However, only one tag responds to its reader at a time. In MSMA, each tag in the view field of the reader is assigned a narrowband subcarrier channel by the reader, then the sensor data can be concurrently streamed using the dedicated subcarriers. An overview of the communication protocol and MSMA tags is explained in the next subsection.

1.1 Communication protocol

Each MSMA tag should be capable of inventory, read, and write operations in Gen2. In addition to the standardized communication protocol, the MSMA tag can handle subsequent subcarrier channel allocation and data streaming (Figure 2). The communication between the reader and MSMA tags includes the following three stages:

■Stage 1 Inventory: During this stage, the interrogator inventory every MSMA tag and also standard Gen2 tags with Gen2 SELECT, QUERY, and related commands. SELECT with a particular session shall be reserved for streaming start at the beginning of Stage 3 in the current implementation. Although the algorithm of the subsequent subcarrier allocation to each MSMA tag depends on the reader's implementation, the collection of received signal strength indicator (RSSI) during the inventory is usually recommended. Our practice is to assign the weak RSSI subcarrier to subcarriers that are close to powering continuous waves [3] to reduce mutual interference caused by harmonics. In this context, the function of subcarrier is to determine the appropriate subcarrier from available subcarrier channels, whereas allocation represents actual instructions between the reader and each tag.

■Stage 2 Subcarrier assignment and allocation: Unique subcarrier is assigned and allocated to each MSMA tag using Gen2 WRITE command to specific memory addresses.

A special frame structure is introduced and explained in the subsequent section to allocate and calibrate the subcarrier frequency produced by an MSMA tag. Our implementation of subcarrier allocation is described in [4]. After the subcarrier allocation, the slave sensor is configured through an SPI. The SPI communication is encapsulated in Gen2 WRITE command.

■Stage 3 Streaming: To start streaming from all MSMA tags, the reader sends a SELECT command of Gen2 with session S3 in the current implemenation. The implementation determines how to continuously retrieve data from the sensor through an SPI.

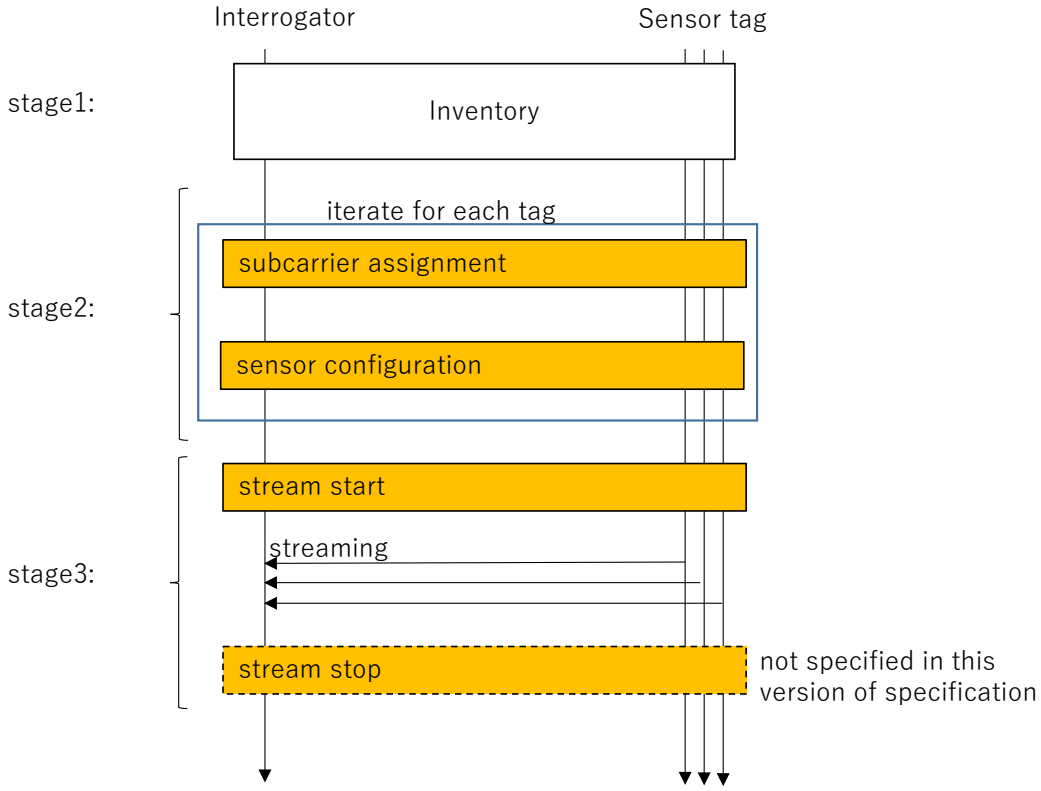

Figure 2 Communication prototype between interrogator and sensor tag. Shaded blocks represent an additional protocol on top of Gen2

2 Communication protocol and sensor control

2.1 Subcarrier frequency and symbol definition

In Stage 3 of communication, one symbol of chip or bit shall be represented with at least two cycles of subcarrier. If a symbol is represented with one cycle of subcarrier, it is baseband coding. The subcarrier frequencies in MSMA comprise integer multiples of base subcarrier frequency (Figure 3). In the figure, three base subcarrier frequencies are denoted by subcarrier 1 with m_s = 1, 2, 3. Notably, this coding is only applied to Stage 3; the standardized Gen2 coding and modulation specified by the reader can be employed in Stages 1 and 2.

For example, when the symbol rate in the streaming phase is 5 kbps and m_s = 2 and no coding is introduced; the frequencies of subcarrier 1, 2, and 3 are 10, 20, and 30 kHz, respectively. When symbol rate is 5 kbps and m_s = 3, the frequencies are 15, 30, and 45 kHz,

respectively. Similarly, the arbitrary bitrate of multiple subcarriers can be realized by adjusting the subcarrier frequency and coding rules.

To facilitate the demodulation in the reader for consecutive zeros or ones, we employ the Miller encoding on top of subcarrier coding in this specification[1].

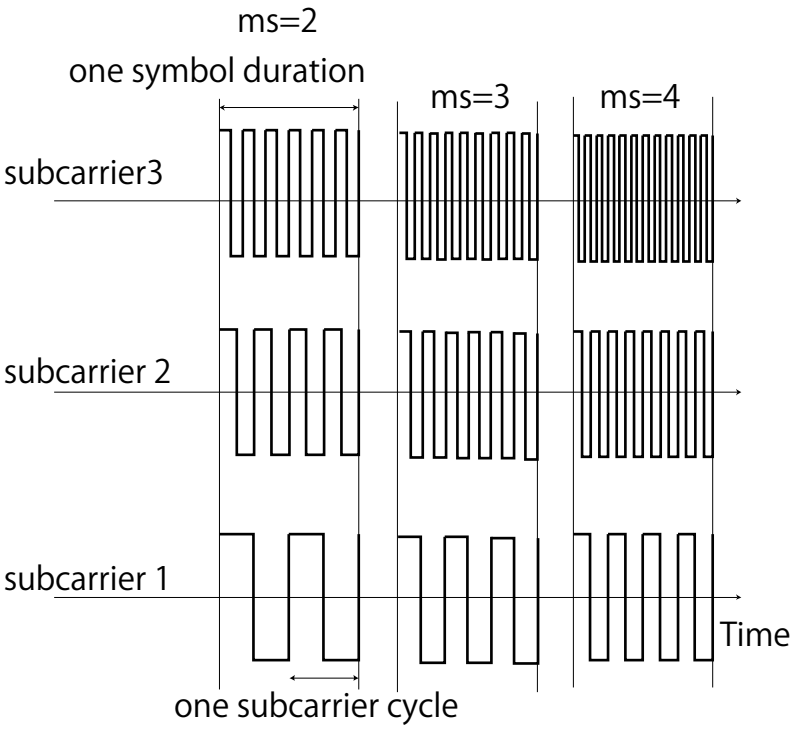

Figure 3 Subcarrier frequency and symbol

The state diagram of Miller encoding is shown in Figure 4.

[1] Convolution coding will be used in the next edition of this extension protocol, which will be disclosed in 2022.

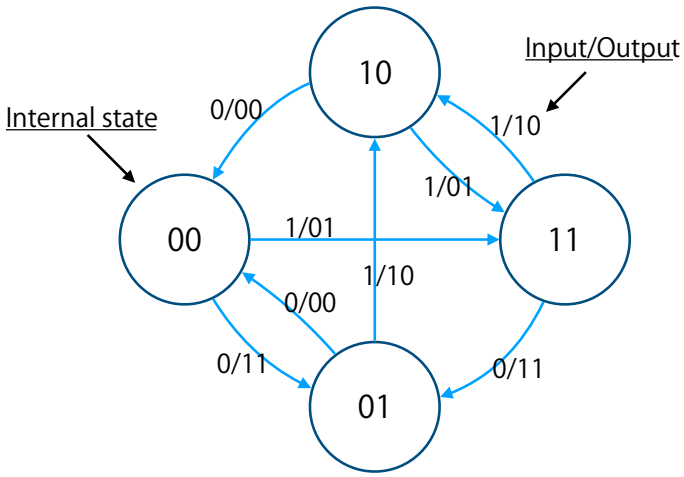

Figure 4 Miller encoding state transition

The subcarrier is XORed with Miller encoded baseband signal, except for the preamble as explained below.

2.2 Streaming frame

An MSMA tag composes a continuous frame (Figure 5) to transfer streaming data to the reader in Stage 3 of the protocol. The leading 5 bits are the preamble without Miller encoding. The rest of the frame shall be encoded with the Miller coding. The CRC-5[2] is generated by convoluting the frame starting from the first bit of zone with the characteristic equation of x^5+x^3+1, Preset b01001. If there is no error in the return link, by applying the same generation polynomial until the end of CRC-5, the residue shall be b00000. This CRC-5 generation is the same as Gen2.

Zone ID is specified by the reader. Sequence ID is the frame ID automatically incremented by one in each frame. The data length N is specified by the reader with STR_CNT register.

Preamble	Zone ID	Sequence ID	Data	CRC5
5 bit equivalent	3 bits	8 bit (0-255 sequential data)	N×8 bits	5 bits
1010101010	001	255		

Figure 5 Return link frame structure in the streaming mode

[2] CRC-16 will be used in the next version of protocol for strong error detection.

2.3 Writing configuration with Gen2 WRITE command

The reader allocates subcarriers to tags and configures sensors using Gen2 WRITE command. The structure of a WRITE command is shown in Figure 6. WordPtr uses Extensible Bit Vectors defined in Gen2. Special register addresses for subcarrier allocation and sensor configuration will be specified.

Write (8bit)	Membank	WordPtr	Data (XORed with handle)	Handle	CRC16
11000011	2 bits (11:user)	(EBV)			16 bits

Figure 6 Gen2 WRITE command

The response from a tag to the reader after receiving a WRITE command is as follows: Upon receiving the WRITE command, a tag responds with the following delayed reply. When an MSMA tag fails to perform the instructed write or configure, it shall reply with Success/Fail = 1 with a proper error code defined in Annex I of [1].

Preamble	Header	Handle/Error code	CRC16
10 bits	1 bit	16 bits	16 bits
4M/BLF + 010111	0: success	handle	
4M/BLF + 010111	1: fail	Error code	

The special user memory addresses to MSMA tag configurations are defined in Table 1.

Table 1 Memory assignment

Memory alias	Description	Memory WordPtr
SPI_WRITE	Write one byte data to SPI	80 H
DCO_CNT	Set subcarrier frequency	81 H

SUB_DIV	Set the division number of the tag clock and the bit rate of the subcarrier	82 H
SPI_INST	Set the WRITE and READ instruction word used in SPI	83 H
STR_CNT	Specify the leading address and the number of bytes of the sensor to read. Zone ID can also be specified with this command	84 H

The register's address in the user memory bank and the word format to be written are defined as follows. The value shall be stored as MSB first byte order[3].

SPI _WRITE (80 H)

The high byte is the address, and the low byte is the data point to be written. The tag uses a sensor-specific WRITE command specified in the SPI_INST register. (0×0A for ADXL362).

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Address								Data							

DCO_CNT (81 H)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	X	C3	C2	C1	C0	M4	M3	M2	M1	M0	F4	F3	F2	F1	F0

SUB_DIV (82 H)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

[3] Original intention was LSB first. This may change in the next edition.

X	X	X	X	X	X	S2	S1	S0	B6	B5	B4	B3	B2	B1	B0

S2, S1, and S0 : Subcarrier divider control words;

bit rate : B0–B6: bit rate divider control words

SPI_INST (83 H)

This word defines the WRITE and READ command code. High 8 bits for WRITE and low 8 bits for READ sensor and RFIC communication are shown in Figure 7; for ADXL362, they are 0×0A and 0×0B, respectively.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0×0A								0×0B							

STR_CNT (84 H)

This word defines the data point to be read from a sensor. The high 8 bits (15:8) is the starting address. Bit 7–4 is the number of bytes to be read, Bit 3 is to select antenna, and Bit 2 is the 0 Zone ID. For ADXL362 to read XDATA, YDATA, ZDATA, TEMP (total 16 × 4 = 64 bits = 8 bytes), the register values are as follows:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Address								# of bytes to read				RFU	ZONE ID		
0×08								1000				0	001		

2.4 Subcarrier allocation and bit rate configuration

Although the design is required to generate subcarrier frequency in an MSMA tag, the recommended way to deliver specified subcarrier frequency with a relatively slow clock rate of the master clock in RFIC is by adjusting the frequency of the oscillator in a tag to be an integer multiple of designated subcarrier frequency. Alternatively, subcarrier frequency can be produced by decimating a single master clock. However, in such a design, a high

subcarrier frequency tends to involve bias, which may violate the subcarrier accuracy requirement.

Because the subcarrier frequency produced by an MSMA tag does not immediately match the specified frequency owing to the instability of the DCO clock, this communication protocol can perform an iterative adjustment (Figure 1). The first SUB_DIV to specify the subcarrier frequency division allows using the iterative adjustment to specify the master clock of an MSMA tag.

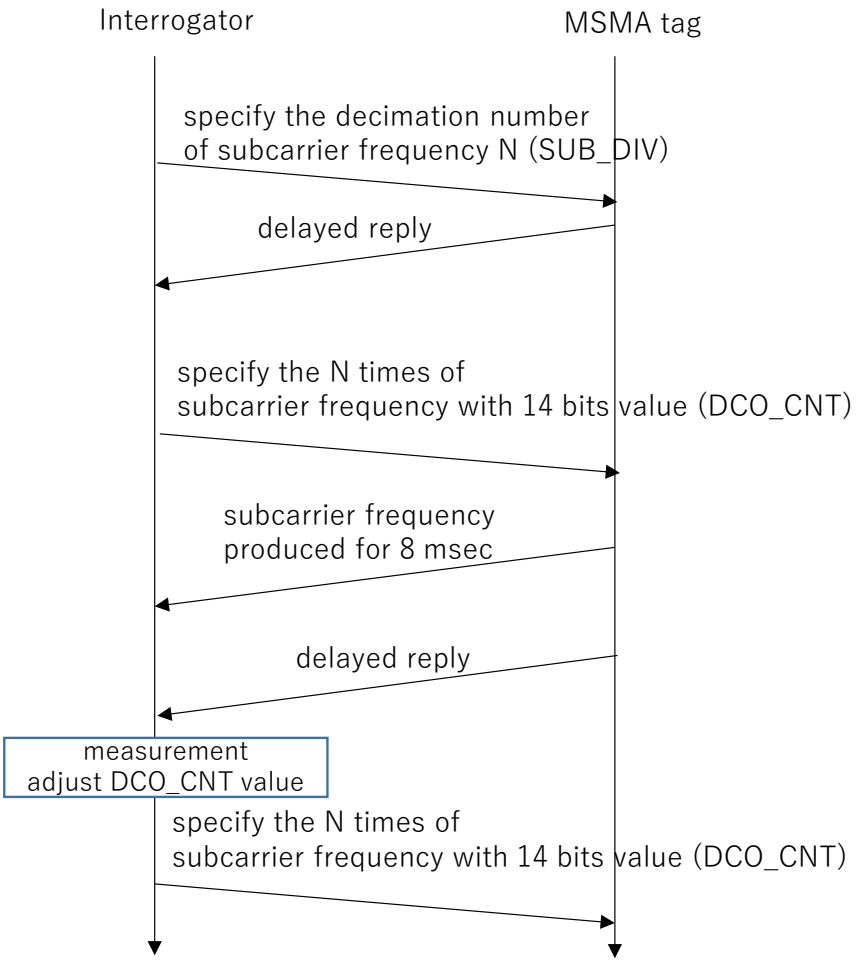

Figure 7 Iterative subcarrier frequency adjustment

The 14-bits DCO value comprises overlapped coarse, middle, and find registers (Figure 8).

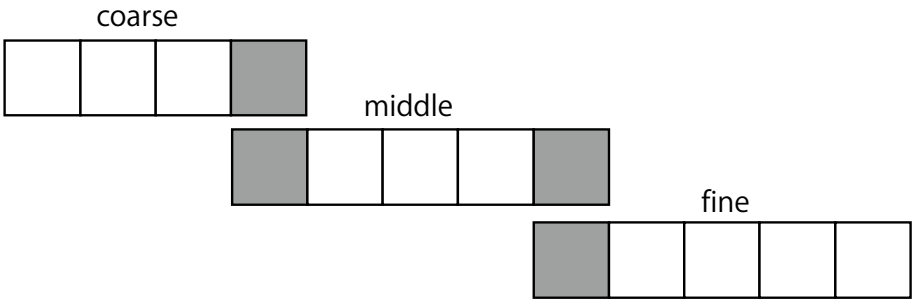

Figure 8 Overlapped DCO_CNT register value

The 14-bit values *X* relates to the actual frequency as follows:

$$f = 400\,X + 691200$$

Consequently, one subcarrier frequency can be represented in general with four patterns of register values, allowing some errors in the adjusting accuracy of DCO (Figure 9).

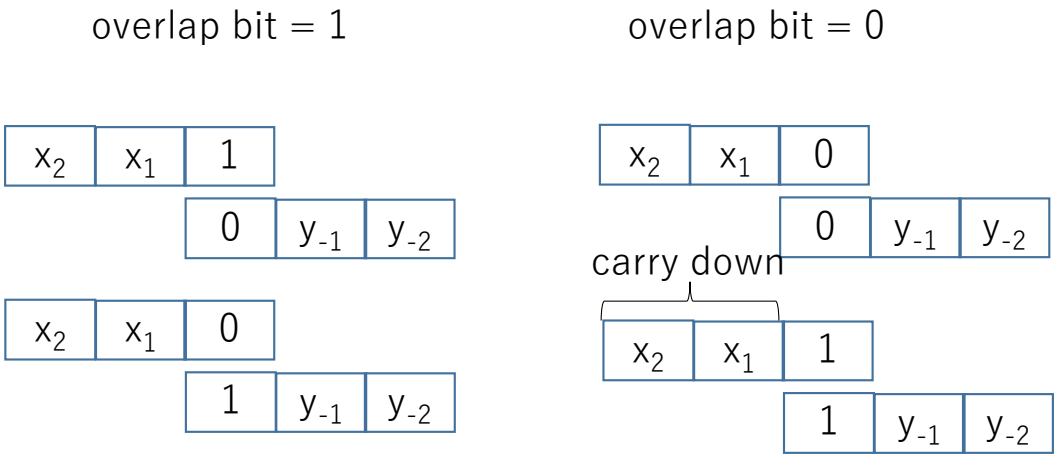

Figure 9 Candidates to represents one overlap bit

However, the increase in the subcarrier frequency against a unit increase in each register value cannot exceed 2.0 because there will be a gap subcarrier frequency that cannot be compensated in such cases (Figure 10).

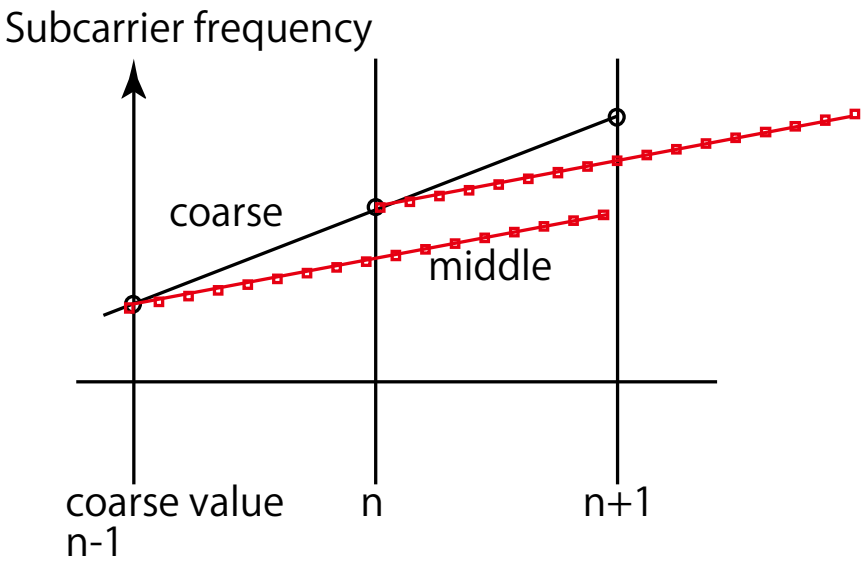

Figure 10 Slopes of each DCO value cannot be different more than two times. This figure is depicted for coarse and middle registers.

The subcarrier and bit rate is illustrated in Table 2.

Table 2 Subcarrier and bitrate allocation

Code (14bits)			DCO Clock (MHz)	dividing ratio	Dividing ratio (3 bits)	sub. Freq (kHz)	100kbps	40kbps	20kbps	10kbps	5kbps
C	M	F									
0100	11011	10000	1.28	32	101	40			0000001	0000010	0000100
0111	11101	10000	1.6	32	101	50					0000101
1010	11111	10000	1.92	32	101	60				0000011	0000110
0011	10010	10000	1.12	16	100	70					0000111
0100	11011	10000	1.28	16	100	80		0000001	0000010	0000100	0001000
0110	10100	10000	1.44	16	100	90					0001001
0111	11101	10000	1.6	16	100	100				0000101	0001010
1001	10110	10000	1.76	16	100	110					0001011
1010	11111	10000	1.92	16	100	120			0000011	0000110	0001100
0010	10101	11000	1.04	8	011	130					0001101
0011	10010	10000	1.12	8	011	140				0000111	0001110
0011	11110	11000	1.2	8	011	150					0001111
0100	11011	10000	1.28	8	011	160		0000010	0000100	0001000	0010000
0101	10111	11000	1.36	8	011	170					0010001
0110	10100	10000	1.44	8	011	180				0001001	0010010
0111	10000	11000	1.52	8	011	190					0010011
0111	11101	10000	1.6	8	011	200	0000001		0000101	0001010	0010100
1000	11001	11000	1.68	8	011	210					0010101
1001	10110	10000	1.76	8	011	220				0001011	0010110
1010	10010	11000	1.84	8	011	230					0010111
1010	11111	10000	1.92	8	011	240		0000011	0000110	0001100	0011000
1011	11011	11000	2	8	011	250					0011001
0010	10101	11000	1.04	4	010	260				0001101	0011010
0010	11011	11100	1.08	4	010	270					0011011
0011	10010	10000	1.12	4	010	280			0000111	0001110	0011100
0011	11000	10100	1.16	4	010	290					0011101
0011	11110	11000	1.2	4	010	300				0001111	0011110
0100	10100	11100	1.24	4	010	310					0011111
0100	11011	10000	1.28	4	010	320		0000100	0001000	0010000	0100000
0101	10001	10100	1.32	4	010	330					0100001
0101	10111	11000	1.36	4	010	340				0010001	0100010
0101	11101	11100	1.4	4	010	350					0100011
0110	10100	10000	1.44	4	010	360			0001001	0010010	0100100
0110	11010	10100	1.48	4	010	370					0100101
0111	10000	11000	1.52	4	010	380				0010011	0100110
0111	10110	11100	1.56	4	010	390					0100111
0111	11101	10000	1.6	4	010	400	0000010	0000101	0001010	0010100	0101000
1000	10011	10100	1.64	4	010	410					0101001
1000	11001	11000	1.68	4	010	420				0010100	0101010
1000	11111	11100	1.72	4	010	430					0101011
1001	10110	10000	1.76	4	010	440			0001011	0010110	0101100
1001	11100	10100	1.8	4	010	450					0101101
1010	10010	11000	1.84	4	010	460				0010111	0101110
1010	11000	11100	1.88	4	010	470					0101111
1010	11111	10000	1.92	4	010	480		0000110	0001100	0011000	0110000
1011	10101	10100	1.96	4	010	490					0110001
1011	11011	11000	2	4	010	500				0011001	0110010
0010	10010	10110	1.02	2	001	510					0110011
0010	10101	11000	1.04	2	001	520			0001101	0011010	0110100
0010	11000	11010	1.06	2	001	530					0110101
0010	11011	11100	1.08	2	001	540				0011011	0110110
0010	11110	11110	1.1	2	001	550					0110111
0011	10010	10000	1.12	2	001	560		0000111	0001110	0011100	0111000
0011	10101	10010	1.14	2	001	570					0111001
0011	11000	10100	1.16	2	001	580				0011101	0111010
0011	11011	10110	1.18	2	001	590					0111011
0011	11110	11000	1.2	2	001	600	0000011		0001111	0011110	0111100
0100	10001	11010	1.22	2	001	610					0111101
0100	10100	11100	1.24	2	001	620				0011111	0111110

A concrete example of subcarrier frequency allocation is explained below.

i. The reader writes to SUB_DIV register as 4 division = b100. The bit rate value in the word does not matter in this particular SUB_DIV.
ii. The interrogator writes to DCO_CNT register with an appropriate frequency value.
iii. The tag replies with the DCO_CNT divided by four subcarrier frequencies for 8 ms.
iv. The reader samples the information regarding 1/4 DCO frequency and issues an updated DCO_CNT value to compensate for the error.

Example:

Assuming an interrogator wants to allocate a 200-kHz subcarrier to an MSMA tag after the inventory, the DCO frequency of the MSMA tag should be 1.6 MHz according to Table 2. For DCO control, the interrogator expects to receive a 400 kHz (1/4 DCO) subcarrier for 8 ms after issuing a DCO_CTL.

i. DCO_CTL is 0111 11101 10000. Suppose that the received subcarrier is 404000 Hz, which is approximately 1% higher than the designated frequency. Interrogator needs to lower the tag's clock by approximately 1%.
ii. The interrogator knows the DCO frequency is 1.6 MHz and the received subcarrier frequency is multiplied by four, yielding 1616 = 404 × 4 kHz, which is 16 kHz higher than the designated frequency. The DCO frequency can be adjusted with 0.4-kHz resolution for 1 bit of DCO fine division (5 bits from LSB).
iii. The bias 16 kHz can be compensated with 16/0.4 = 40 = 0 × 28 = b0010 1000, which is subtracted from the original DCO_CNL = 0111 11101 10000, yielding 0111 11100 01000.

2.5 Sensor configuration

Depending on the sensor type, sensor configuration is needed through SPI by writing to SPI_WRITE register. Example configuration for Analog device ADXL362 is illustrated in Annex A.

2.6 Sensor data streaming SPI interface exchange

An MSMA chip will collect sensor data through SPI, and plug the data into the streaming frame. Data is collected by providing the SPI clock synchronizing to the radio interface

bitrate. Consequently, the buffer between SPI and the backscatter baseband can be minimized.

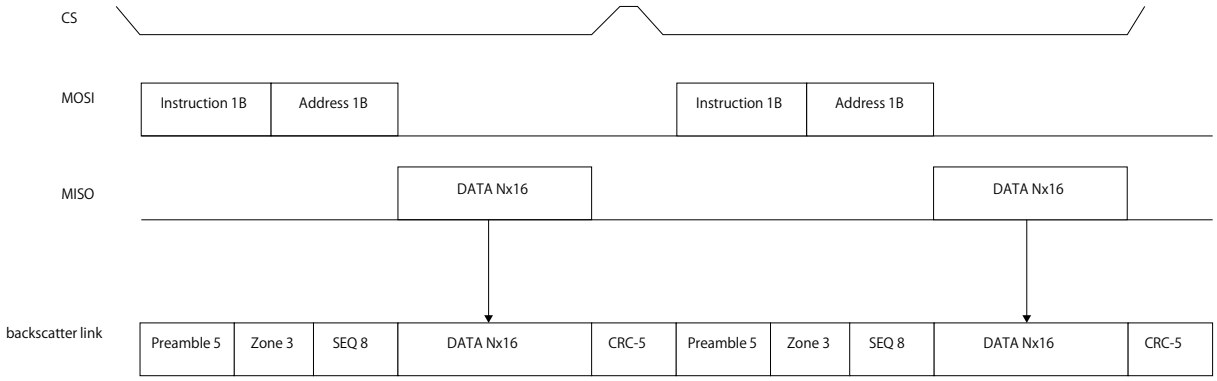

Figure 11 Sensor data encapsulation in the streaming stage

2.7 Start streaming

Start streaming is implemented using a special SELECT command (Session S3 is used as the target of the SELECT command) because SELECT is processed by all tags in the view field without producing any response[4].

Select the Zone ID by SELECT command specifying the user memory address 1 to obtain the following:

Select	Target	Action	Membank	Pointer	Length	Mask	Truncate	CRC
4	3	3	2	EBV	8	Variable	1	16
1010	011	000-101	11(User)	0000 0000	0000 0011	Zone ID	0	CRC-16

Figure 13 Selecting target tags before streaming

Notably, SELECT can only be applicable to EEPROM (00H-07H).

[4] In the next edition of this extension, An RFU command will be used for start and stop streaming.

2.8 Stream stop

To stop streaming, we just stop providing CW from the interrogator. Further control will be considered in the next edition of this extension.

3 Reference

[1]. "ISO/IEC 18000-63, Information Technology–Radio frequency identification for item management-, Part 63 parameters for air interface communications at 860 MHz to 960 MHz type C," 2015.

[2]. J. Mitsugi, Y. Kawakita, K. Egawa, and H. Ichikawa, "Perfectly synchronized Streaming from multiple digitally modulated backscatter sensor tags," IEEE Journal of Radio Frequency Identification, vol. 3, no. 3, pp. 149-156, Sept. 2019, doi: 10.1109/JRFID.2019.2914246.

[3]. Nitish Rajoria, Yuki Igarashi, Jin Mitsugi, Yusuke Kawakita, and Haruhisa Ichikawa, "Comparative analysis on channel allocation schemes in multiple subcarrier passive communication system," IEICE TRANSACTIONS on Communications Vol.E98-B No.9 pp.1777-1784, (2015). DOI: 10.1587/transcom.E98.B.1777.

[4]. Kuanfeng Tang, Chao Zhang, Maodong Wang, Xu. Shengliang, Ji. Shujiang, Na Yan, Hao Min, and Jin Mitsugi. "A novel method to improve the subcarrier frequency accuracy for UHF RFID sensing system," In IEEE RFID 2021 (Virtual Event,USA). pp.1-6, (2021), doi=10.1109/RFID52461.2021.9444388.

Acknowledgement

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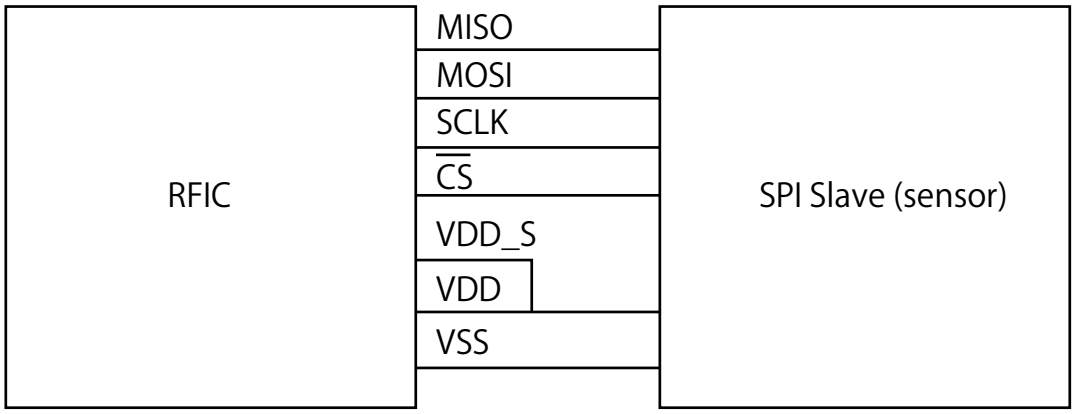
A. Guideline of ADXL362 configuration through Gen2 WRITE commands

a. Prerequisite

Data streaming from ADXL362 with MSMA tag requires the following configuration using Gen2 memory WRITE commands. The example connection between the RFIC and ADXL362 is shown in Figure 14.



PAD name	category	Type	Output/Input	Value
MISO	SPI	Digital	Input	high：1.6~2.5V, low：0
MOSI		Digital	Output	high：1.6~2.5V, low：0
SCLK		Digital	Output	high：1.6~2.5V, low：0
VSS	Signal GND	Power	Input/Output	0
VDD_S	SPI output voltage regulation	Digital	Input	
VDD		Power	Output	1.4V~2V
Antenna N		RF antenna N		
Antenna P		RF antenna P		

Figure 14 RFIC, ADXL362, and Interrogator interface diagram

Before any GEN2 READ/WRITE command issuance, SPI READ/WRITE commands (for ADXL362, they are 0×0B and 0×0A, respectively) shall be registered to RFIC by issuing a WRITE to SPI_INST(83 H = EBV10000011) of user memory (bank 11) such that to obtain the following:

WRITE	Membank	WordPtr	Data	Handle	CRC-16
11000011	11	10000011	16 bits XOR with handle	16 bits	16 bits

b. Writing to ADXL register

A Gen2 WRITE command to a specific user memory (address 0×80 = EBV 10000000) in user memory bank (bank 11) received by the RFIC passes through to the SPI using the registered WRITE command. For example, if we write a byte data point (0×aa) to a specific address of ADXL (0×77), the WRITE command is as follows.

WRITE	Membank	WordPtr	Data	Handle	CRC-16
11000011	11	10000000	16 bits (0×77aa) XOR with Handle	16 bits	16 bits

After receiving the WRITE command, tag responds with a delayed reply, which comprises a sequence of specified subcarrier of 43-bit duration.

Preamble	Success/Fail	Handle	CRC16
10 bits	1 bit	16 bits	16 bits
4M/BLF + 010111	0: success 1:Error		

c. Reading from RFID memory

We can read data in RFIC memory with Gen2 READ command to obtain the following:

READ	Membank	WordPtr	WordCount	Handle	CRC-16
11000010	2 bit	EBV	8 bits	16 bits	16 bits

Tag reply to a successful READ is as follows:

Header	Memory Words	Handle	CRC-16
1	Variable	16 bits	16 bits

For example, when we READ SPI_INST (83H) for one word, the Gen2 READ command is as follows:

READ	Membank	WordPtr	WordCount	Handle	CRC-16
11000010	11	10000011	00000001	16 bits	16 bits

In the current edition of the extension, we cannot read the register value of an SPI sensor. However, in the next edition of the extension, we enable the function.

d. Popular configuration parameters

The followings are the configuration of ADXL applied in our experiments.

Description	SPI address	Data example	Note
Sensor activation threshold value setting (lower byte)	0×20	0×96	Data is the direct reading of acceleration level that activates MEMS sensor. 0×96 = 150-mg activation.
Sensor activation threshold value (higher byte)	0×21	0×00	The threshold level can be specified with 11-bit data.
Activity measurement duration	0×22	0×01	To avoid false triggering, several samples are used to distinguish activate/inactivate. The absolute time is determined by DATA/output data rate (ODR). ODR is defined in Filter Control (0×2C) register.
Activate/Inactivate	0×27	0×01	Activity Enabled = 0×01, otherwise 0×00, activity is not detected. The sensor is

control			always on and consumes power. Engaging inactivity by defining inactive threshold level can be a viable option.
FIFO control	0×27	0×00	FIFO disabled. The sensor data is retrieved by RFIC and stream to the interrogator by consecutively issuing SPI_READ (0×0B) command by RFIC.
Filter control	0×2C	0×45	The acceleration range and ODR. 0×05 = max 2 g and 200 Hz 0×45 = max 4 g and 400 Hz
Power control	0×2D	0×02	0×00: standby (low power consumption:10 nA) 0×02: measurement

The streaming data length and Zone ID can be configured by writing the following one word data

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Starting address								# of bytes to read				RFU	Zone ID		

The address to retrieve data (12-bit data LSB) are as follows:

0x0E	XDATA_L	[7:0]
0x0F	XDATA_H	[7:0]
0x10	YDATA_L	[7:0]
0x11	YDATA_H	[7:0]
0x12	ZDATA_L	[7:0]
0x13	ZDATA_H	[7:0]
0x14	TEMP_L	[7:0]
0x15	TEMP_H	[7:0]

The example data to read XDATA, YDATA, ZDATA, TEMP (total 16 × 4 = 64 bits = 8 bytes) and Zone ID = 1 is as follows.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

0×0E	1000		001

This 16-bit value (0×0e81) shall be written to STR_CNT (0×85) in the user memory bank with WRITE command the such that

WRITE	Membank	WordPtr	Data	Handle	CRC-16
11000011	11	10000101	16 bits (0×0e81) XOR with Handle	16 bits	16 bits

B. On the SPI communication with Analog Device ADXL 362

Acceleration and temperature sensor data in ADXL362 are updated with the sampling frequency specified in the FILTER_CNT register (0×2C) ODR bits.

Besides using FIFO, acceleration data XDATA, YDATA, ZDATA, and temperature data TEMP can be read with Burst READ (0×0B) from the corresponding register 0×0E-0×0F, 0×10-0×11, and 0×12-0×13, 0×14-0×15, respectively, each with 12-bit data and 4-bit padding. The register value is updated with ODR bits such as 400 Hz = 2;5 ms at the maximum. The required bit rate to send N consecutive samples of the specified axis data can be calculated by assuming the following backscatter frame:

Preamble	Zone	Sequence ID	Data	CRC5
4-bit equivalent	3 bits	8 bits (0-255 sequential data)	N × 16-bits	5 bits
10101010				

Assuming the bit rate in the air interface to be X kbps, the maximum time to retrieve data from sensor through SPI is 85/X ms (Figure 15).

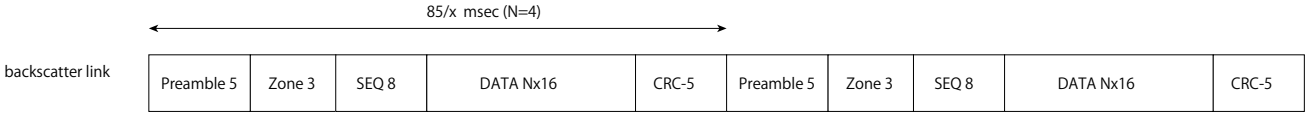


Figure 15 Maximum time to collect sensor data through SPI. For 5 kbps, the maximum time is 17 ms.

Assuming N = 4, to collect XDATA, YDATA, ZDATA, and temperature yielding a total of 8 bytes, there are 85 bits to be transferred over the air interface. In SPI communications, the number of data that shall be collected before the data streaming demands additional two bytes to specify the SPI reading (0×0B) and the leading address (0×0E) is shown in Figure 16.

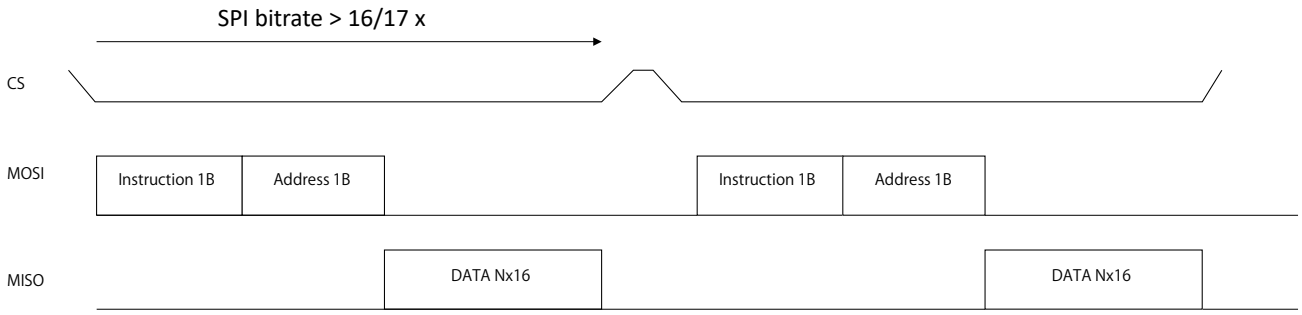


Figure 16 Data transfer between RFIC and sensor through SPI

C. Revision History

Date	Version	Note
June 15, 2021	1.0	Initial version
July 1, 2021	1.1	Editorial and format change
July 7, 2021	1.2	Editorial change